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Step by Step Design Procedure of a Distribution Static Synchronous Compensator (DSTATCOM)

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Abstract

DSTATCOM is one of the power conditioning devices that is used to mitigate power quality problems in distribution systems. The overall performance of the DSTATCOM is strictly related with the proper selection of power circuit configuration and controller algorithm. The power circuit of DSTATCOM consists of dc link capacitor, inverter and passive filter. The control circuit of DSTATCOM consists of reference signal extraction, DC link voltage control, AC voltage control and switching signal generation. Compensating current reference signal is generally derived from the measured quantities by the use of the Instantaneous Symmetrical Component Theory (ISCT) and dq theory based method. A proportional–integral (PI) controller is generally used to maintain a constant voltage at the dc-link of a Voltage-Source Inverter (VSI). Furthermore, by connecting a delta connected inductor-capacitor-inductor (LCL) passive filter at inverter output, the high order harmonics generated by the DSTATCOM can be easily and effectively eliminated. This study presents the design procedures for power and control circuits of 300 kVA DSTATCOM in detail.

Keywords: Distribution static synchronous compensator, Power circuit, Control circuit, Power quality.

Bir Dağıtım Sistemi Statik Senkron Kompanzatörün (DSTATKOM) Adım Adım Tasarım Prosedürü

Özet

DSTATKOM, dağıtım sistemlerinde güç kalitesi problemlerini düzeltmek için kullanılan güç iyileştirici cihazlardan biridir. DSTATKOM' un performansı tamamıyla güç devresinin ve kontrolcü algoritmasının uygun seçimiyle ilgilidir. DSTATKOM'un güç devresi DA bara kapasitöründen, doğrultucudan ve pasif filtreden oluşur. DSTATKOM'un kontrol devresi referans sinyal çıkartımından, DA bara gerilim kontrolünden, AA gerilim kontrolünden ve anahtarlama sinyali üretiminden oluşur. Kompanze eden akım referans sinyalleri genellikle Anlık Simetrik Bileşen Teorisi (ASBT) ve dq teori tabanlı metot kullanarak ölçülen değerlerden üretilir. Gerilim kontrollü doğrultucuda (GKD) DA barayı sabit gerilimde tutmak için

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genellikle PI kontrolcüsü kullanılır. Ayrıca, doğrultucu çıkışına üçgen bağlı bobin-kondansatör-bobin (BKB) pasif filtresi bağlayarak, DSTATKOM tarafından üretilen yüksek dereceli harmonikler kolayca ve etkin bir şekilde yok edilmektedir. Bu çalışma, detaylı olarak 300kVA DSTATKOM'un güç ve kontrol devreleri için tasarım prosedürlerini sunmaktadır

Anahtar Kelimeler: Dağıtım sistemi statik senkron kompanzatörü, Güç devresi, Kontrol devresi, Güç kalitesi

1. INTRODUCTION

Power quality is defined as the concept of powering and grounding electronic equipment in a manner that is suitable to the operation of that equipment and compatible with the premise wiring system and other connected equipment in Institute of Electrical and Electronics Engineers (IEEE) Standard 1159-1995 [1]. Power quality problems in industrial applications concern a wide range of disturbances, such as voltage sags and swells, flicker, interruptions, harmonic distortions etc. To solve these problems, several different Custom Power devices have been proposed. The term Custom Power has been defined as "the concept of employing power electronic (static) controllers in 1kV through 38kV distribution systems for the purpose of supplying a compatible level of power quality necessary for adequate performance of selected facilities and processes" [2].

Distribution Static Compensator (DSTATCOM) is one of the custom power devices, a shunt compensation device which is generally used to solve power quality problems in distribution systems. The main advantage of DSTATCOM is that, it has a very sophisticated power electronics based control which can efficiently regulate the current injection into the distribution bus. The second advantage is that, it has multifarious applications, e.g. canceling the effect of poor load power factor, suppressing the effect of harmonic content in load currents, regulating the voltage of distribution bus against sag/swell etc, compensating the reactive power requirement of the load and many more [3]. The applications of the DSTATCOMs into the renewable and distributed energy systems are the trend topics in the DSTATCOM literature [4-7].

The performance of DSTATCOM depends on the design of power circuit components, control algorithm used to extract the reference current signals and switching scheme to generate the gate signals. Classification and topologies of DSTATCOM are reported by various researchers in [8,9]. These are classified based on the types of inverter topology as voltage source inverter (VSI) and current source inverter (CSI). In a D-STATCOM, either a VSI having a capacitor in the dc link and series reactors on the ac side or a CSI having a reactor in the dc link and shunt-connected capacitors on the ac side can be employed. Among these, VSI is the most common choice in DSTATCOM applications [10]. The DSTATCOM topologies can be classified based on the number of switching devices, use of transformers for isolation, use of transformers for neutral current compensation, etc. These DSTATCOMs are developed to meet the requirements of different applications such as single-phase two-wire [11], three-phase three-wire and three-phase four-wire distribution systems. The topologies for the three-phase three-wire DSTATCOMs are classified as three-leg VSI [12] and two-leg VSI with split capacitors [13]. The topologies for the three-phase four-wire DSTATCOMs are mainly classified as two split capacitor (2C) [14], four-leg (4L) [15] and three H-bridge (3HB) [16] and etc. In the literature, different types of transformer connection for the neutral current compensation are reported as star-delta [17], zigzag [18] and T-connection [19] and so on.

The performance of a DSTATCOM strictly depends on its reference current signal generation techniques. There are many control algorithms reported in the literature for control of DSTATCOM such as instantaneous reactive power

theory [20], synchronous reference frame theory [21], instantaneous symmetrical components based [22], fast Fourier transform (FFT) [23], neural network (NN) based theory [24], etc. Generation of suitable switching signal is the most significant part of DSTATCOM's control and has a high influence on the compensation performance [25]. PWM is the most reliable way of reconstructing a desired output voltage waveform. PWM methods are often categorized as open loop (feed-forward) and closed loop (feed-back) methods. The open loop method is subdivided into sinusoidal PWM (SPWM) [18,19] and space vector PWM (SVM) [26]. The closed loop method are classified into hysteresis current control [27] and linear current control involving ramp comparison [28], predictive [29], deadbeat [30], sliding mode [19], linear quadratic regulator [31], etc. Apart from these methods the selective harmonic elimination technique [10] also used for generation proper switching signal.

This paper aims to provide a comprehensive design procedure of DSTATCOM. This paper is organized as follows: First, the operation principles of DSTATCOM are presented in Section 2. Section 3 illustrates the design of DSTATCOM on power circuit structure and control circuit structure. Finally in Section 4, conclusions of this study are explained.

2. OPERATION PRINCIPLES OF DSTATCOM

Figure 1 shows the schematic representation of the DSTATCOM and the single phase equivalent circuit of a power system with a DSTATCOM is shown in Figure 2. The V_I, $V_{Coupling}$, V_{PCC} and V_S represents the DSTATCOM output voltage; the voltage drop caused by coupling impedance, PCC voltage and source voltage, respectively.

In this arrangement, the steady-state power exchange between the device and the AC system is mainly reactive. Regulating the amplitude of the DSTATCOM output voltage controls the reactive power exchange of the DSTATCOM with the AC system. If the amplitudes of V_I and V_{PCC} are equal, the reactive current is zero and the DSTATCOM does not generate/absorb reactive power. If the amplitude of V_I is increased above the amplitude of V_{PCC}, the current flows through the transformer reactance from the DSTATCOM to the AC system and the device generates reactive power (capacitive). If the amplitude of V_I is decreased to a level below that of V_{PCC}, then the current flows from the AC system to the DSTATCOM, resulting in the device absorbing reactive power (inductive) [32,33].

Also by proper adjustment of the phase angle between the DSTATCOM output and the utility grid voltages, the DSTATCOM can manage active power flow with the utility grid. This exchange can be used to mitigate the internal losses of the inverter and to maintain the DC capacitor charged to the proper DC voltage hereby adjusting the DSTATCOM output voltage magnitude. Figure 3 presents the steady state vector diagram of DSTATCOM at fundamental frequency for the transition states from inductive to capacitive mode and vice versa. The transition from capacitive to inductive mode is obtained by shifting the angle δ from zero to a positive value. The active power is transferred from the DC capacitor to the utility grid and causes a voltage drop in the DC link. The transition from inductive to capacitive mode is obtained by shifting the angle δ from zero to a negative value. The active power is transferred from the utility grid to the DC capacitor and causes a rise in the DC link voltage [34].

The exchange of active and reactive power between DSTATCOM and utility grid can be calculated by Equation (1) and (2).

$$P = \frac{V_{PCC}\, V_I}{X_{Coupling}} \sin \delta \tag{1}$$

$$Q = \frac{V_{PCC}^2}{X_{Coupling}} - \frac{V_{PCC}\, V_I}{X_{Coupling}} \cos \delta \tag{2}$$

There are several factors that must be considered when designed the DSTATCOM and associated control circuits. In relation to the power circuit the following issues are of major importance:

- DC link capacitor size
- Output filter equipment
- Inverter equipment

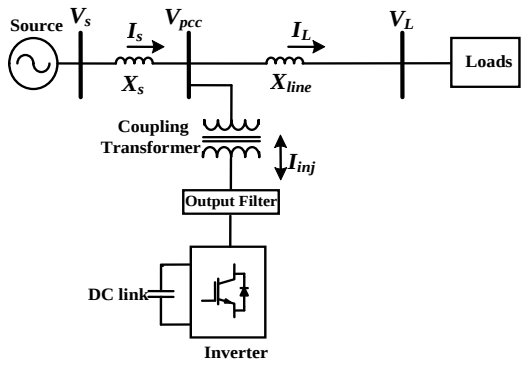

Figure 1. Schematic diagram of DSTATCOM

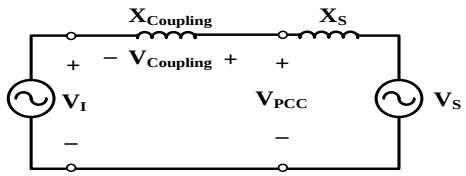

Figure 2. Single-phase equivalent circuit of a power system with a DSTATCOM

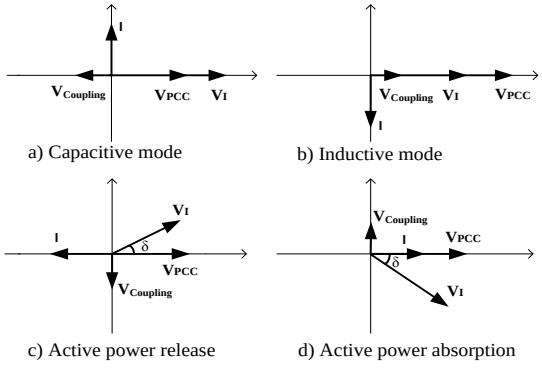

Figure 3. Vector diagram of DSTATCOM

3. DESIGN OF DSTATCOM

The DSTATCOM system consists of two groups: power circuit and control circuit.

1. Power Supply
2. Loads
3. DSTATCOM
   a. Power Circuit : (Voltage Source Inverter; DC Link; Interface Filter)
   b. Control Circuit : (Reference Current Generation; Current Control)

3.1. Power Supply

Power supply is a wye connected $400V_{L\text{-}L}$ at 50 Hz. For modeling the grid a symmetrical three-phase voltage source having an inductance and resistance is used.

3.2. Loads

The most important issue to be considered when a DSTATCOM is designed, total characteristic of nonlinear loads which are connected point of common connection is to be made reactive power compensation and harmonic filtering. The nonlinear load block is a three-phase fully controlled thyristor bridge rectifier feeding DC load. Loads are designed as linear and nonlinear with wye-connected three-phase three-wire systems and total rating of 300kVA (0.8 pf.). The model of the linear and nonlinear load block is shown in Figure 4.

Voltage drop occurs at PCC during switching commutation at the thyristor rectifier. The reason of this is disconnect currents of line inductances at phase immediately. Therefore, in line commutated thyristor rectifier, while passing from a phase to another phase, three thyristor transmission occurs simultaneously. Two of this three thyristors by-passes the line to line voltage which they are connected at PCC. In this case, in order to prevent the emerging line voltage notches, choke inductances is connected AC inputs of thyristor and diode rectifier. According to German VDE standards, the voltage drop on the choke inductance should be more than 5% of line-neutral voltage at the maximum fundamental load current.

$$wL_d I_L \geq 0.05 \frac{V_{LL}}{\sqrt{3}} \tag{3}$$

w : fundamental frequency (rad/s)

L_d : choke inductance (H)
I_L : fundamental load current (A)
V_{LL} : line to line voltage (V)

Choke inductance value is calculated as $L_d \geq 0.085mH$ using (3) when $V_{LL} = 400V, I_L =$ 433A and *w* = 314.16 rad/s . The choke inductance is selected as 0.3mH.

3.3. DSTATCOM Power Circuit Configuration

3.3.1. Design of Voltage Source Inverter

The inverter circuit converts DC power to AC power. Three-phase IGBT with anti-paralleling diodes having turn-off capability are used in the inverter circuits. A voltage source inverter is energized by a capacitor at the input. The inverter is then connected in parallel to the distribution line through interface filter (LCL) as shown in Figure 5. The interface filter establish a link between VSI and power system.

The voltage source inverter used in DSTATCOM makes the harmonic control possible. This inverter uses a DC capacitor as the supply and can switch at a high frequency to generate a signal which will cancel the harmonics from the nonlinear load. The current waveform for canceling harmonics is achieved with the VSI and an interface filter. The interface filter converts the voltage signal created by the inverter to a current signal. The desired waveform is obtained by accurately controlling the switches in the inverter. Control of the current wave shape is limited by the switching frequency of the inverter and by the available driving voltage across the interface filter. The driving voltage across the interface filter determines the maximum *di/dt* that can be achieved by the filter. This is important because relatively high values of *di/dt* may be needed to cancel higher order harmonic components [35].

3.3.2. Design of DC Link

A DC capacitor provides constant DC link voltage. The output voltage of the DSTATCOM is generated by the VSI operated from a DC-link capacitor. The DC-link capacitor has direct influence on the harmonic distortion of the output voltage generated by the DSTATCOM and speed of response of the controller. If the capacitor is undersized the controller's response will be fast but the DC-link voltage will have excessive ripple and consequently the output voltage will contain high levels of harmonic distortion. Moreover, high transient overshoots will exists. On the other hand, an oversized capacitor will improve the output voltage waveform shape and reduce the transient overshoots but at the expense of a sluggish controller's response [34]. A PI controller is used to control the DC-link voltage. If care is not taken in the adjustment of the PI parameters, the system may become unstable.

According to the above analysis, the selection of capacitor voltage (V_{dcref}) and capacitance of the capacitor value C_{DC} can be determined from (4) and (5),

$$V_{dcref} = \frac{2\sqrt{2}\,V_{LL}}{\sqrt{3}m_a} \tag{4}$$

$$C_{dc} = \frac{3S_n nT}{(1.8V_m)^2 - (1.4V_m)^2} \tag{5}$$

where V_{dcref} is the reference capacitor voltage, V_{LL} is line to line grid voltage, m_a is the modulation index, C_{dc} is the DC capacitor value, V_m is peak value of grid voltage, S_n is power rate of system, *T* is system time period, *n* is the cycle that starts working the controller.

Reference DC-link voltage is estimated as 680V using (4) when m_a=1 and $V_{LL} = 400V$. DC-link capacitor value is calculated as 66 mF using (5) when $V_m = 326.6V$, $S_n = 300kVA$, $n = 0.5$ and $T = 0.02s$. The capacitor is selected as 60mF.

3.3.3. Inverter Output Filter

3.3.3.1. L filter

The L filter (Figure 6) is the first order filter with attenuation 20 dB/decade over the whole

frequency range. Although a single inductor L filter is popular and simple use, it has a low attenuation and high inductance value. The voltage drop across the inductor makes a poor system dynamics, hence causing a long-time response.

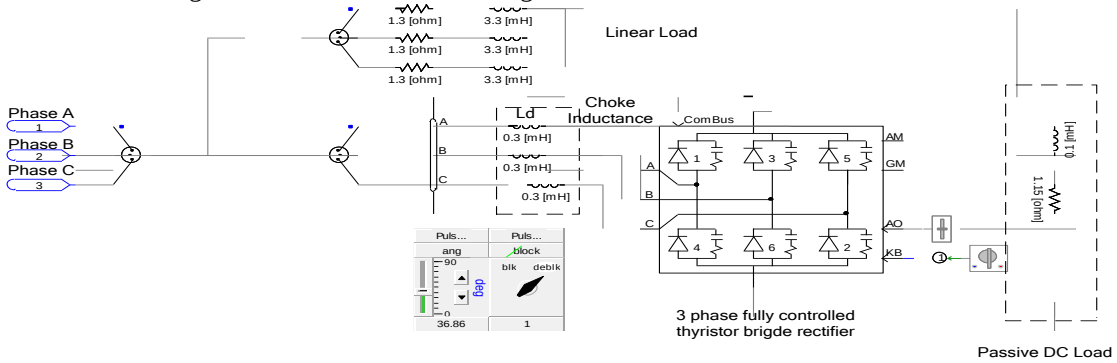

Figure 4. PSCAD model of the linear and nonlinear load

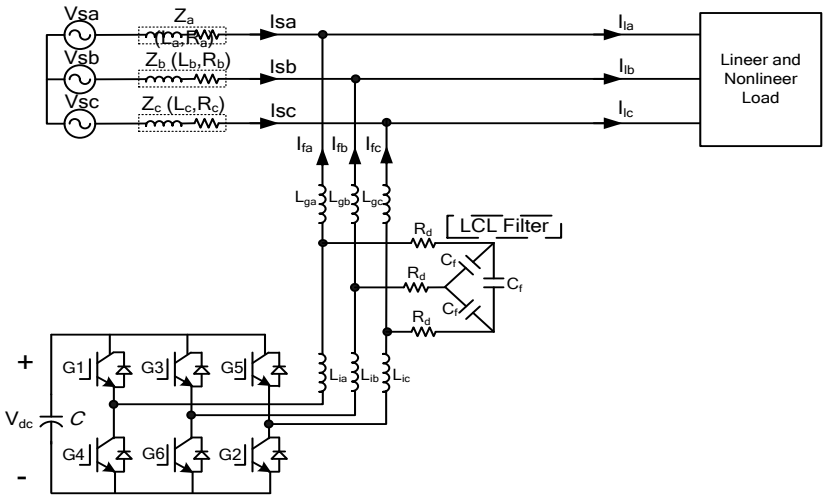

Figure 5. Diagram illustrating components of the DSTATCOM

By using L filter, the inverter switching frequency must have a high value in order to sufficiently attenuate the harmonics [36,37].

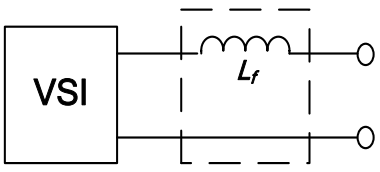

Figure 6. Circuit diagram of L filter

Peak ripple current is chosen to be the criterion for designing the inductor. For calculating the ripple current, no-load condition is considered and the effect inductor resistance is assumed to be negligible. Under this condition, the inverter reference voltage is equal to the supply voltage. Thus the required smoothing inductance given by [38]:

$$L_f = \frac{V_{dc}}{6 f_{sw} \Delta_{ph(p-p)max}} \quad (6)$$

where $\Delta_{ph(p-p)max}$= 15% of peak compensation current, V_{dc} is the supply voltage of inverter (DC link voltage) and f_{sw} is the switching frequency. The smoothing inductance is calculated as 0.17 mH using (6) when V_{dc} = 680V , $\Delta_{ph(p-p)max}$= 65A and f_{sw} = 10kHz. To improve the smoothing inductance performance in simulation study, the inductance is selected as 0.15mH.

3.3.3.2. LCL Filter

The attenuation of the LCL filter is 60 dB/decade for frequencies above resonant frequency. Therefore lower switching frequency for the inverter can be used. Namely, the high frequency harmonics in voltage and current, generated by the high frequency switching in the VSI, can be suppressed by the use of a LCL filter. LCL filter consists of two inductors in series and a capacitor shunted between them. Compared to a filter with the use of a single inductor, the damping of the switching harmonics, at lower switching frequency, improve by using a LCL filter. The total inductance of the filter should be as small as possible to realize fast tracking and high dynamics, and still handle the ripple in the current [39]. Wye connected LCL filters are generally used in systems, but delta connected LCL filter is used in this study as shown Figure 7. If inductances and capacitances are the same for a delta connected LCL filter and a wye connected LCL filter, resonant frequency of a delta connected LCL filter is decreased to 3 times resonant frequency of a wye connected LCL filter. So, there are more reduced harmonics in capacitor currents in case of a delta connected LCL filter than a wye connected LCL filter. As switching frequency is lower to a few kilohertz, these harmonics cause to distort inverter control signals. This is advantageous to control an inverter with a delta connected LCL filter because currents flowing into wye connected capacitors have harmonic components with larger magnitude [40]. Applying Kirchhoff's current and voltage laws to Figure 7, differential equations can be achieved. These are (7) for paths between the inverter side and the filter, (8) for paths between the filter and the grid side, (9) at capacitors in the filter [40].

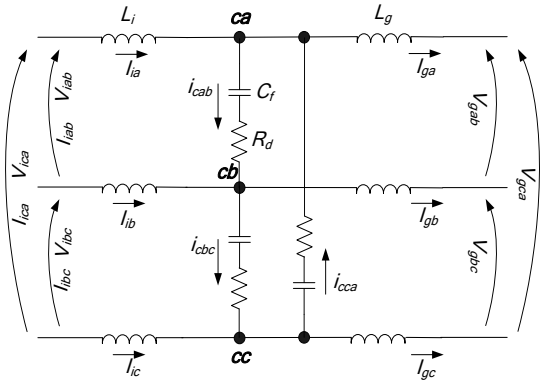

Figure 7. Circuit diagram of LCL Filter

V_{iab}, V_{ibc}, V_{ica} : inverter line-to-line voltages
V_{gab}, V_{gbc}, V_{gca} : grid line-to-line voltages
V_{cab}, V_{cbc}, V_{cca} : potential voltage between node *ca*, *cb* and *cc*
I_{ia}, I_{ib}, I_{ic} : inverter line currents flowing from the inverter side to the filter
I_{ga}, I_{gb}, I_{gc} : grid line currents flowing from the filter to the grid side
I_{iab}, I_{ibc}, I_{ica} : phase currents calculated from I_{ia}, I_{ib}, I_{ic}
I_{cab}, I_{cbc}, I_{cca} : capacitor currents
ca, *cb*, *cc* : nodes at capacitors

$$-\begin{bmatrix} V_{iab} \\ V_{ibc} \\ V_{ica} \end{bmatrix} + 3L_i \frac{d}{dt}\begin{bmatrix} I_{iab} \\ I_{ibc} \\ I_{ica} \end{bmatrix} + \begin{bmatrix} V_{cab} \\ V_{cbc} \\ V_{cca} \end{bmatrix} = 0 \quad (7)$$

$$-\begin{bmatrix} V_{cab} \\ V_{cbc} \\ V_{cca} \end{bmatrix} + 3L_g \frac{d}{dt}\begin{bmatrix} I_{gab} \\ I_{gbc} \\ I_{gca} \end{bmatrix} + \begin{bmatrix} V_{gab} \\ V_{gbc} \\ V_{gca} \end{bmatrix} = 0 \quad (8)$$

$$C_f \frac{d}{dt}\begin{bmatrix} V_{cab} \\ V_{cbc} \\ V_{cca} \end{bmatrix} - R_d C_f \frac{d}{dt}\begin{bmatrix} I_{cab} \\ I_{cbc} \\ I_{cca} \end{bmatrix} = \begin{bmatrix} I_{cab} \\ I_{cbc} \\ I_{cca} \end{bmatrix} \quad (9)$$

It is supposed that $[V_{iab}\ V_{ibc}\ V_{ica}]' = V_i$, $[V_{gab}\ V_{gbc}\ V_{gca}]' = V_g$, $[V_{cab}\ V_{cbc}\ V_{cca}]' = V_c$, $[I_{iab}\ I_{ibc}\ I_{ica}]' = I_i$, $[I_{gab}\ I_{gbc}\ I_{gca}]' = I_g$, $[I_{cab}\ I_{cbc}\ I_{cca}]' = I_c$

where symbol $'$ means transpose. Equation (7), (8) and (9) are transformed to (10) by the Laplace transform theorem on the assumption that all initial values of the state variables are zero. Then, desired transfer functions $I_c(s)/V_i(s)$, $V_c(s)/I_c(s)$ and $I_2(s)/(V_c(s) - V_g(s))$ can be calculated from (10) to represent the system. The equation (11) is the proposed mathematical model of the system.

$$\begin{bmatrix} -V_i(s) + s\,3L_i I_i(s) + V_c(s) = 0 \\ -V_c(s) + s\,3L_g I_g(s) + V_g(s) = 0 \\ sC_f V_c(s) = (1 + sC_f R_d) I_c(s) \end{bmatrix} \quad (10)$$

$$\begin{bmatrix} G_1 = \dfrac{I_c(s)}{V_i(s)} \\ = \dfrac{s^2 3L_g C_f}{s3(L_i + L_g) + s^2 3C_f R_d (L_i + L_g) + s^3 9L_i L_g C_f} \\ G_2 = \dfrac{V_c(s)}{I_c(s)} = \dfrac{1 + sC_f R_d}{sC_f} \\ G_3 = \dfrac{I_g(s)}{V_c(s) - V_g(s)} = \dfrac{1}{s3L_g} \end{bmatrix} \quad (11)$$

The first-harmonic, low order harmonic and high order harmonic current could be got by decomposing the output current of inverter. As shown in Figure 7, the current ripple is decreased because of inductance L_i that the current flow through. The capacitance is features low resistance to high order harmonic, but the inductance is features high resistance, so the high order harmonic can only flow through capacitance. Then the left current of first-harmonic and low order harmonic flow through inductance L_g into power grid [41]. Parameters design of the inductors in LCL filter is based on the principle as follows [42]:

1. The voltage drop at the inductors of LCL filter must be less than 10% of the phase voltage of the grid

$$w(L_i + L_g)I_n < 10\% * U_n/\sqrt{3} \Rightarrow$$

$$\Rightarrow (L_i + L_g) < 0.17mH$$

2. In order to limit the short circuit current and the harmonic current, the inductance of inductors should not be too small. The minimum value of inductance is determined by the ripple current which is chosen between 10%-20%.

$$20\% * 8 * (L_i + L_g)I_n f_{SW} \geq V_{DC} \Rightarrow$$

$$\Rightarrow (L_i + L_g) \geq 0.098\ mH$$

In conclusion, the value range of inductance of the inductors in LCL filter is

$$0.0098\ mH \leq L_i + L_g < 0.17\ mH$$

The value of inductance is chosen as 0.1 *mH*. So the inductance values are

$$L_i = 0.07\ mH, \qquad L_g = 0.03\ mH$$

In order to guarantee the efficiency of DSTATCOM, reactive power absorbed by filter capacitors must be less than 5% of rated capacity.

$$C \leq \frac{5\%\ S_n}{3w\left(\frac{U_n}{\sqrt{3}}\right)^2} \Rightarrow C \leq 0.3\ mF$$

The value of capacitance for star connection is chosen as 0.25 mF. Delta connection capacitance value is estimated as 0.083 mF.

For making the harmonics current flow through the filter capacitors as more as possible. The resonant frequency of LCL filter should avoid appearing in low or high frequency band and parameters design should meet the following requirements.

$$X_c = (0.1 : 0.2)X_{Lg}$$

$$10f_n < f_{res} < f_c/2 \Rightarrow 0.5\ kHz < f_{res} < 5\ kHz$$

Test as follows:

$$\frac{X_c}{X_{Lg}} = \frac{1}{w_c^2 C L_g} = 0$$

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_i + L_g}{3L_i L_g C}} = 2.2\ kHz$$

Damping Resistance: The equivalent impedance of the passive LCL filter approaches zero at the resonance frequency and it will consequently lower the stability margin of the system down. To avoid instability, a resistor R_d is used in series with the capacitor. The resistance R_d is normally selected in proportion to the capacitive reactance of the filter at the resonance frequency ($1 / (3 * 2\pi f_{res} C)$). This resistance can be chosen such that it minimizes the power dissipation too [43]. Comparison of L and LCL filter performances based on various parameters is presented in Table 1.

Table 1. Comparison of L and LCL filters

Parameters	L filter	LCL filter
Switching ripple in percentage (terminal voltages, source currents)	high	low
Value of L for ripple percentage in filter currents	large	small
Source neutral current	high	low
Compensation performance in terms of %THD	good	good
Current controller complexity	less	relatively more

3.4. DSTATCOM Control Strategy

3.4.1. Reference Current Generation

DSTATCOM control is accomplished by monitoring the three phase line currents to the linear/nonlinear loads and the three phase line-to-neutral voltages at the load bus, and then generating the three phase reference currents that should be supplied by the voltage source inverter. In this simulation study compensating current reference signal is derived from the measured quantities by the use of the Instantaneous Symmetrical Component Theory (ISCT) and Synchronous Reference Frame (SRF) based method. When the compensating currents are detected, they are used as a reference signal in the inverter current control loop and thus compared with the real voltage source inverter current to generate the switching control signals.

Firstly, the method of ISCT is used to simplify analysis of unbalanced three-phase power systems under both normal and abnormal conditions. The purpose of this theory is to perform balanced source current and harmonic free. For extract the current reference signal, the positive sequence of current extract by the ISCT. The transformation is defined as:

$$\begin{bmatrix} V^+ \\ V^- \\ V^o \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \times \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

Here V^+, V^- and V^o denote the positive, negative and zero sequences respectively and the complex number a is

$$a = e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$$

$$a^2 = e^{j\frac{4\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$$

The inverse of this transformation is:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \times \begin{bmatrix} V^+ \\ V^- \\ V^o \end{bmatrix}$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \times \begin{bmatrix} V^+ \\ V^- \\ V^o \end{bmatrix}$$

The instantaneous positive-sequence components are defined as

$$\begin{bmatrix} V_a^+ \\ V_b^+ \\ V_c^+ \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix} \times \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

The instantaneous negative-sequence components are defined as

$$\begin{bmatrix} V_a^- \\ V_b^- \\ V_c^- \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} \times \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

The instantaneous zero-sequence components are defined as

$$V_a^0 = V_b^0 = V_c^0 = \frac{1}{3}(V_a + V_b + V_c)$$

Secondly, ABC components of extracted positive sequences are transformed to the orthogonal and stationary $\alpha\beta$ frame system by used the Clarke transformation. The equation of Clarke transformation is given in Equation (12).

$$i_{\alpha\beta}(t) = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \quad (12)$$

Next step, the stationary components of the currents convert to direct (d) and quadrature (q) components by Park's transformation. The values of DQ transformation are calculated using (13). The phase angle θ defines the fundamental frequency phase information of the utility voltage and it is obtained from a phase locked loop circuit which is investigated.

$$i_{dq} = \frac{2}{3}\begin{bmatrix} cos\,\theta & sin\,\theta \\ -sin\,\theta & cos\,\theta \end{bmatrix}\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} \quad (13)$$

$$i_{dq} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta-120) & \cos(\theta+120) \\ \sin\theta & \sin(\theta-120) & \sin(\theta+120) \end{bmatrix}\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \quad (14)$$

If three-phase parameters such as currents and voltages are balanced, the value of the DQ transformation results in DC constant values. In addition, the resulting DC values make voltage controller design easier. Figure 8 shows three-phase voltages and their dq-axis values for the balanced voltage sag. Figure 9 shows the resulting DQ values. It is clearly shown that regardless of the voltage sag, the value in d-axis remains zero, and the q-axis component instantaneously indicates the change of the voltage magnitude. The DQ transformation uses instantaneous values.

Therefore, the detection time is much faster than other methods such as average, RMS and peak detection. However, for the unbalanced voltage sag, this DQ transformation method does not show the instant change of DC values [44].

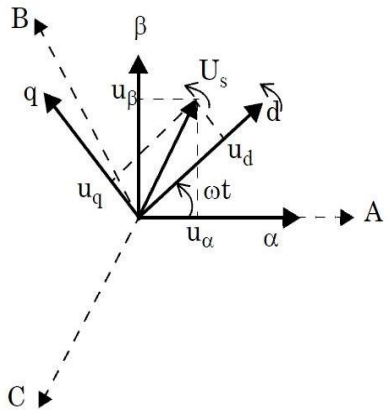

Figure 8. αβ and DQ rotating frame vector representation

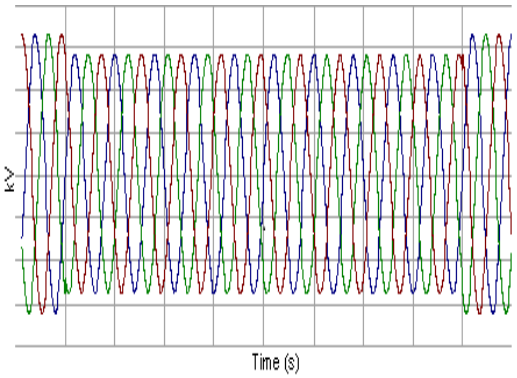

Figure 9. The result of DQ transformation of balance three phase voltage

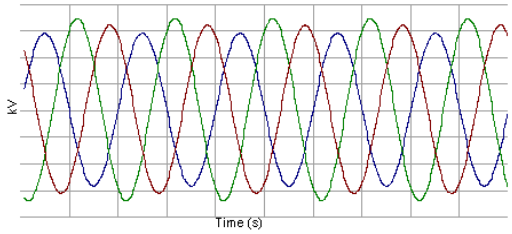

Figure 10. The result of DQ transformation of unbalance three phase voltage

3.4.2. AC Voltage Controller

To control the magnitude of the voltage at PCC, an AC voltage controller using reactive power injection is used. Injection of reactive current at PCC results in a change of the voltage magnitude due to the variation of the voltage drop over the impedance of the system at PCC. V_{ac} is compared with the pre-defined reference value V_{ref}. The error signal is fed to the PI block to generate the small signal oscillation is limited to suppress the variation in the output. Figure 11 describes the structure of AC voltage controller.

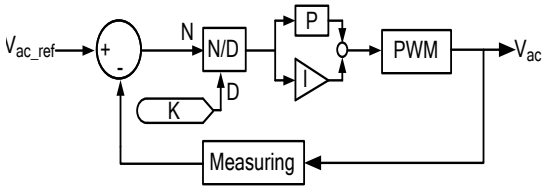

Figure 11. The structure of AC voltage controller

3.4.3. DC Link Voltage Controller

What happens actually is that the DC bus loses some of its energy to compensate for the energy losses of the system and in this process its voltage starts to drop. As the voltage tries to drop, the voltage controller acts and maintains the DC bus voltage constant by absorbing active power from the grid. Thus, the voltage controller indirectly uses the DC bus voltage to supply the energy losses of the system from the grid [45].

The DC side voltage V_{dc} is measured and compared with the reference voltage side V_{dcref}, and the error signal is fed to PI controller. Figure 12 describes the structure of DC voltage controller.

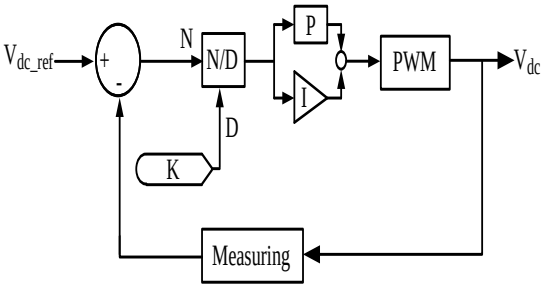

Figure 12. The structure of DC link voltage controller

3.4.4. Sinusoidal PWM Current Controller

The sinusoidal pulse-width modulation (SPWM) technique produces a sinusoidal waveform by filtering an output pulse waveform with varying width. A high switching frequency leads to a better filtered sinusoidal output waveform. The desired output voltage is achieved by varying the frequency and amplitude of a reference or modulating voltage. The variations in the amplitude and frequency of the reference voltage change the pulse-width patterns of the output voltage but keep the sinusoidal modulation. A low-frequency sinusoidal modulating signal is compared with a high frequency triangular signal, which is called the carrier signal. The switching state is changed when the sine waveform intersects the triangular waveform. The crossing positions determine the variable switching times between states [46]. In three-phase SPWM is used as gate signal generation for VSI as shown Figure 13. The switching pulses are generated by comparing the reference current compensation signal I_{error} with a fixed frequency carrier triangular wave and the relative levels of the wave forms are used to control the switching of the devices in each phase leg of the inverter. And the frequency of the triangular wave is set to f_{tri} = 10kHz. The overall control structure of DSTATCOM using PWM is shown in Figure 14.

The parameters of the designed DSTATCOM are listed in Table 2.

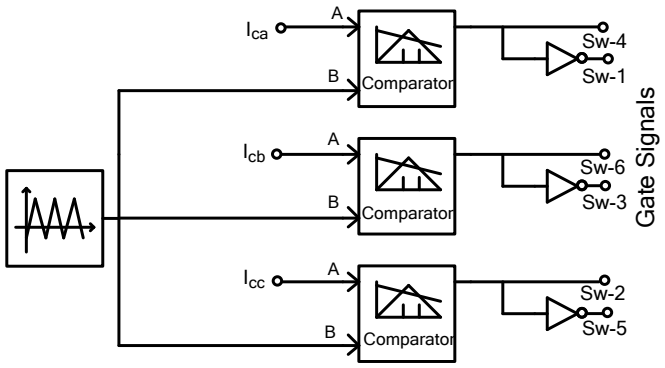

Figure 13. Generation of PWM gate signals

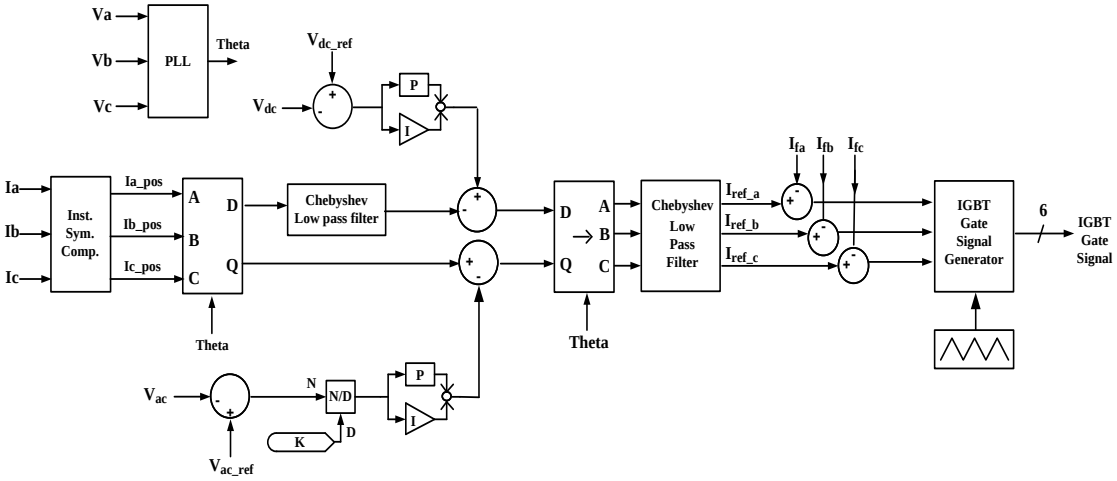

Figure 14. The overall structure of DSTATCOM

4. CONCLUSIONS

DSTATCOM can mitigate many types of power quality disturbances. The proper selection of power circuit configuration and control algorithms are essential for DSTATCOM design. In this study, step by step design procedure of 300 kVA DSTATCOM has been proposed. The design procedure is detailed in two parts, power circuit and control circuit. The guidelines for the design of the power and control circuits of DSTATCOM are illustrated in detail. All the design of the DSTSTCOM system can meet the power quality requirement given in IEEE Standard 519-1992. This paper helps the researchers to select the optimum control strategies and power circuit configuration for DSTATCOM applications.

5. ACKNOWLEDGEMENT

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- Project title/number: Design and Simulation of DSTATCOM for Power Quality Improvements, MMF2013YL15.

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Table 2. The parameters of the designed DSTATCOM

System Parameters	
Voltage source	400V
Fundamental frequency	50 Hz
Impedance of feeder	R=0.02 Ω, X=0.16 mH
Nonlinear load	A three-phase diode rectifier that supplies a load of 1.15 + *j*0.0314Ω
Linear load	R= 1.3 Ω, X=3.3 mH
DC link voltage	680V
DC link capacitor	60 mF
Switching frequency	10 kHz
LCL filter	L_i=0.07 mH, L_g=0.03 mH, C_f=0.083 mF, R_d=0.8 Ω
Resonance frequency of filter	2.2 kHz
DC Link PI Controller Parameters	
Proportional gain	50
Integral time constant	0.5 s
AC Voltage PI Controller Parameters	
Proportional gain	100
Integral time constant	0.05 s

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